

Customer No.: 31561
Application No.: 10/605,254
Docket No.: 9676-US-PA

IN THE CLAIMS

Please amend the claims as follows.

1. (currently amended) A method of fabricating of a flash memory, comprising:
sequentially forming a tunneling dielectric layer, a conductive layer and a mask layer on a substrate;

patterning the tunneling dielectric layer, the conductive layer and the mask layer ~~into to form a plurality of strips strip structure;~~

performing an ion implantation step to form a buried drain region in the substrate between the strips;

~~patterning the strip structure to form a control gate structure, in which the patterned conductive layer is further patterned into a floating gate;~~

forming an insulation layer between the strips ~~on a sidewall of the floating gate structure, the insulation layer having such that a top surface of the insulation layer is between a lower surface and than a top surface of the floating gate patterned conductive layer~~ such that a part of a sidewall of the ~~floating gate patterned conductive layer~~ is exposed;

removing the patterned mask layer;

forming a gate dielectric layer on the top surface and the exposed sidewall of the ~~floating gate patterned conductive layer;~~ and

forming a control gate on the gate dielectric layer.

2. (currently amended) The method according to Claim 1, wherein the step of forming the insulation layer between the strips further comprises:

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forming an insulation material layer on the substrate to cover the ~~floating-gate structures~~ strips and to fill space between the strips ~~floating-gate structures~~;

removing a part of the insulation material layer that covers the ~~floating-gate structures~~ ~~to expose~~ the strips until the patterned mask layer is exposed; and

removing a part of the remaining insulation layer until the top surface of the remaining insulation material layer is between a top surface and a bottom surface of the patterned conductive layer ~~floating-gate structures~~.

3. (currently amended) The method according to Claim 2, ~~further comprising~~ forming wherein the insulation material layer with comprises silicon oxide, silicon nitride, or spin-on glass.

4. (currently amended) The method according to Claim 2, ~~further comprising~~ wherein the insulation material layer is formed by using high-density plasma chemical vapor deposition process ~~for forming the insulation layer~~.

5. (currently amended) The method according to Claim 4, ~~further comprising~~ wherein the high-density plasma chemical vapor deposition process is carried out using tetra-ethyl-oxy-silicate and ozone.

6. (currently amended) The method according to Claim 2, ~~further comprising~~ ~~using chemical mechanical or etch back to remove~~ wherein the step of removing the part of the insulation material layer is accomplished using a chemical mechanical or etch back process.

7. (currently amended) The method according to Claim 2, ~~further comprising~~ ~~using etch back to remove~~ wherein the step of removing the part of the remaining

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insulation material layer is accomplished using an etch back process.

8. (currently amended) The method according to Claim 1, ~~further comprising~~
~~forming wherein~~ the mask layer ~~with~~ comprises silicon oxide or silicon nitride.

9. (currently amended) The method according to Claim 8 ~~1~~, ~~further comprising~~
wherein the step of removing the patterned mask layer is accomplished by using wet
etching process to remove the mask layer.

10. (currently amended) The method according to Claim 8 ~~9~~, ~~further comprising~~
wherein the wet etching process is carried out using phosphoric acid as etchant to
~~remove the mask layer~~ when the mask layer ~~is made of~~ comprises silicon nitride.

11. (currently amended) A method of fabricating a flash memory, comprising:
forming a tunneling dielectric layer and a floating gate on a substrate;
~~forming a buried drain region in the substrate between the floating gates;~~
performing an ion implantation step to form a buried drain region in the
substrate between the floating gates; and

forming an insulation layer ~~on a sidewall of~~ between the floating gates ~~gate after~~
~~forming the floating gates, the insulation layer having a top surface level between a top~~
~~surface and a bottom surface of the floating gate;~~

removing a portion of the insulation layer such that a top surface of the
insulation layer is located between a top surface and a bottom surface of the floating
gates;

forming a gate dielectric layer over ~~on~~ the top surface and the exposed ~~sidewall~~
sidewalls of the floating gates ~~gate~~; and

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forming a control gate on the gate dielectric layer.

12. (currently amended) The method according to Claim 11, wherein the step of forming the insulation layer further comprises:

forming an insulation material layer on the substrate to cover the floating gates gate and to fill space between the floating gates;

removing a part of the insulation material layer that covers the floating gates gate to expose the top surface of the floating gates gate; and

removing a part of the remaining insulation material layer until the top surface of the insulation material layer is between the top surface and the bottom surface of the floating gates gate.

13. (currently amended) The method according to Claim 12, ~~further comprising~~ forming wherein the insulation material layer with comprises silicon oxide.

14. (currently amended) The method according to Claim 13, ~~further comprising~~ wherein the step of forming the insulation material layer is carried out by using high-density plasma chemical vapor deposition process for forming the insulation layer.

15. (currently amended) The method according to Claim 14, ~~further comprising~~ wherein the high-density plasma chemical vapor deposition process is carried out using tetra-ethyl-oxy-silicate and ozone.

16. (currently amended) The method according to Claim 12, ~~further comprising~~ the step of removing the part of the insulation material layer is accomplished by using chemical mechanical or etch back process to remove the part of the insulation layer.

17. (currently amended) The method according to Claim ~~1~~ 11, further

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comprising a step of forming a patterned mask layer on the floating gates ~~gate~~ ~~when the part of the insulation layer formed subsequently is removed by chemical mechanical polishing; and a step of removing the mask layer before forming the gate dielectric layer, wherein the mask layer is made of a material different from that of the insulation layer.~~

18. (currently amended) The method according to Claim 18, ~~further comprising~~ wherein the patterned mask layer is removed during the step of removing the part of the insulation material layer using a wet etching process ~~to remove the mask layer.~~

19. (currently amended) The method according to Claim 12, ~~further comprising~~ wherein the step of removing the part of the remaining insulation material layer is accomplished by using an etch back process ~~to remove the part of the insulation layer.~~